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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,693	07/29/2004	Rishi BHOOSHAN	TI-37087	4692

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EXAMINER
KIK, PHALLAKA

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,693	BHOOSHAN ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004 and 09 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *13-24 and 37-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 25-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20060615*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the Application filed on 7/29/2004 and interview conducted on 6/9/2006. Claims 1-48 are pending, wherein claims 13-24,37-48 are withdrawn from consideration as being directed to non-elected inventions without traverse.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12,25-36, drawn to a method/computer readable medium for determining approximately whether a design of a module violates a design criteria, classified in class 716, subclass 5.

II. Claims 13-21,37-45, drawn to a method/computer readable medium for determining whether a plurality of efuse cells contained in a module can be programmed by applying an appropriate voltage level across each of the plurality of efuse cells, classified in class 714, subclass 4.

III. Claims 22-24,46-48, drawn to a method/computer readable medium of analyzing a module to determine signal characteristics of an output path of the module, classified in class 716, subclass 4.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions I, II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombinations I,II or III

have separate utility such as performing the particular recited functions. See MPEP § 806.05(d).

4. Because these inventions are independent or distinct for the reasons given above and the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Jim Brady (Reg. No. 32,080) on 6/9/2006 a provisional election was made without traverse to prosecute the invention of group I, claims 1-12,25-36. Affirmation of this election must be made by applicant in replying to this Office action. Claims 13-24,37-48 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Objections

7. **Claims 1-12,25-36** are objected to because of the following informalities:

As per **claims 1,25**, "the form" (lines 3,5 respectively) should be --a form-- for proper antecedent basis; "said plurality" (lines 12,16 respectively) should be --a plurality-- for proper antecedent basis; --the transistors-- (or alternatively, --the paths--) should be inserted after "width" (lines 17 and 21, respectively) to clearly indicate which

width refers to. For examination purposes, either the width of the transistors or the paths are assumed.

As per **claims 8,32**, "the form" (line 2) should be --a form-- for proper antecedent basis.

As per **claims 11,35**, --from said layout file further-- should be inserted after "determining" (line 4) to distinguish from "the determination" recited in claims 1,25 from which the claims respectively depend. Also, as per **claim 35**, --said actions-- should be inserted before "further" (line 1) to clearly provide for the missing structural/functional relationships among the elements of the claim.

As per **claim 12**, --of-- should be inserted before "iterations" (line 3) for proper grammar.

As per **claim 26**, "computer readable medium" (lines 4-5) should be --actions-- to clearly provide for the missing structural/functional relationships among the elements of the claim.

As per **claim 29**, "further comprises" (lines 1-2) should be --said actions further comprise-- to clearly provide for the missing structural/functional relationships among the elements of the claim and for proper grammar due to the proposed changes.

As per **claim 30**, --and said actions-- should be inserted before "further" (line 2) to clearly provide for the missing structural/functional relationships among the elements of the claim.

As per **claims 2-12,26-36**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-8,25-32** are rejected under 35 U.S.C. 102(b) as being anticipated by **Itazu et al.** (U.S. Patent No. 6,405,354).

As per **claims 1,25**, all of the elements of the claims are illustrated in Figs. 5-6, wherein the extraction of the topology of the design are performed in steps S1 to S10 (see also col. 5, line 11 to col. 6, line 39) wherein the power network includes resistors and the temporary cells include transistors (see col. 1, lines 32-44; col. 6, lines 40-48); wherein the model generation including replacing the transistors (i.e., temporary cells) with current source and computing the magnitude of the current sources are further described in steps S11 to S14 (see col. 6, line 40 to col. 7, line 6) wherein since the resistances and current sources are based in part on the width or size of the wirings and/or transistors (col. 6, lines 40-48; col. 5, lines 23-33; col. 8, lines 24-33), the magnitude of the current sources are accordingly correspond to some proportion of the width of the wirings and/or transistors; wherein the analysis including the determination if the design violates the desired criteria are further described in steps S15 to S16 (col. 7, lines 7-23); wherein the computer readable medium carrying one or more sequences

of instructions for performing these steps are further described in col. 2, lines 60-65 (see also col. 4, line 55 to col. 5, line 6).

As per **claims 2-3,5,26-27,29**, all of the elements of claims 1,25, from which the respective claims depend, are discussed in the rejection of claims 1,25 above, wherein the further criteria of using the current density and supply voltage drop to ensure that they do not exceed the desired amount are described in col. 7, lines 7-23, wherein such maximum values (i.e., standard values) are further described in 1, line 54 to col. 2, line 7; wherein such cells or modules are rejected when a re-layout is executed.

As per **claims 4,28**, all of the elements of claims 3,27, from which the respective claims depend, are discussed in the rejection of claims 3,27 above, wherein the treatment of the transistors being connected parallel are illustrated in Figs. 2 and 15 in which the current sources, representing the transistors, are analyzed as being connected in parallel.

As per **claims 6,30**, all of the elements of claims 5,29, from which the respective claims depend, are discussed in the rejections of claims 5,29 above, wherein since the "modules" comprises many cells and wirings, the analysis of the modules are accordingly performed at a higher level (i.e., chip-level analysis).

As per **claims 7,31**, all of the elements of claims 6,30, from which the respective claims depend, are discussed in the rejections of claims 6,30 above, wherein since the models are generated based estimated values and extraction values (see col. 6, lines 40-67), such models are accordingly performed using some sort of simulation tool.

As per **claims 8,32**, all of the elements of claims 3,27, from which the respective claims depend, are discussed in the rejections of claims 3,27 above, wherein such layout file would necessarily be provided in order to store the particular cell arrangements/interconnections of the circuit layout for the analysis (see col. 5, line 10 to col. 6, line 35).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 9-12,33-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Itazu et al.** (U.S. Patent No. 6,405,354) in view of **Djaja et al.** (U.S. Patent No. 6,405,160).

As per **claims 9-12,33-36**, **Itazu et al.** disclose all of the elements of claims 1,25, from which the respective claims depend, as discussed in the rejections of claims 1,25 above. However, **Itazu et al.** failed to particular apply such circuit design analysis of the chip-level design comprising transistors and resistors to memory circuits, involving the particular memory array with row arrangements as claimed. **Djaja et al.** disclose a method/system for designing memory array having row arrangements (see col. 2, line 41 to col. 3, line 12) which takes into account current density, and further make use of

locations/coordinates of transistors to keep track of the critical features of the device layout (see col. 4, lines 8-55). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further adapt the method/system of **Itazu et al.** to analyze the memory array circuits as taught by **Djaja et al.** because such adaptation would allow the particular memory circuits as taught by **Djaja et al.** to be verified for proper functionality.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 8:30AM-7PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phallaka Kik
Primary Examiner
Art Unit 2825
June 21, 2006